REMARKS

The Office Action dated February 7, 2006, has been received and carefully noted. The above amendments and the following remarks are being submitted as a full and complete response thereto.

By this amendment, Claims 16, 20, and 26 have been amended. New Claim 27 has been added. The Applicants submit that the claim amendments are fully supported in the specification as originally filed, for example, in Fig. 3, and on page 10, line 15, to page 11, line 8, and that no new matter has been added. Accordingly, Claims 16 to 27 are currently pending in the application and are subject to examination.

Objection to the Claims

Claim 20 is objected to for containing informalities. The Applicants have amended Claim 20 responsive to this objection, as suggested in the Office Action. As such, Applicants respectfully request withdrawal of the objection to Claim 20.

Rejection of Claims 16-23 and 25 Under 35 U.S.C. § 103(a)

Claims 16-17 and 20-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda (U.S. Patent Application Publication No. 20001/0054135) and Akamatsu et al. (U.S. Patent No. 5,983,331, hereinafter "Akamatsu"). Claim 18 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda, Akamatsu and Smith (U.S. Patent No. 6,085,317). Claim 19 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda, Akamatsu and Prouty et al. (U.S. Patent No. 6,470,433, hereinafter "Prouty"). Claims 22 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda, Akamatsu and Takeda (U.S. Patent Application

Publication No. 2001/0011311). Claims 24 and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda, Akamatsu and Suzuki (U.S. Patent Application Publication No. 2003/0070049). Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuda, Akamatsu and Funaba et al. (U.S. Patent Application Publication No. 2002/0159284). To the extent these rejections remain applicable to the claims currently pending, the Applicant respectfully traverses the rejections.

Claim 16, as amended, recites a common memory controller capable of controlling different types of memory chips which are connected to a common bus, comprising a first interface portion for receiving a control output signal to access said memory chips from a controller, and outputting a control input signal to the controller, a conversion control portion for converting said control output signal into a memory input signal in response to a specification of each of said memory chips to which the memory controller is connected, and converting a memory output signal output from the memory chips into the control input signal receivable to the controller, a second interface portion for outputting the memory input signal and receiving the memory output signal, and a plurality of terminals coupled to the second interface portion for connecting the second interface portion to the different types of memory chips via said common bus.

Claim 26 recites a multi chip package comprising a system LSI chip including a common memory controller capable of controlling different types of memory chips which are connected to a common bus, and memory chips coupled to the system LSI chp, and controlled by the common memory controller, the common memory controller including a

first interface portion for receiving a control output signal to access the memory chips from a controller of the LSI chip, and outputting a control input signal to the controller, a conversion control portion for converting the control output signal into a memory input signal in response to a specification of each of the memory chips, and converting a memory output signal from the memory chips into the control input signal receivable to the controller, a second interface portion for outputting the memory input signal and receiving the memory output signal, and a plurality of terminals coupled to the second interface portion, for connecting the second interface portion to the different types of memory chips via the common bus.

The Applicant submits that the applied prior art fails to teach or suggest all the elements of amended Claims 16 and 26. Specifically, the Applicant submits that the applied prior art fails to teach or suggest at least the combination of features including a common memory controller capable of controlling **different types of memory chips which are connected to a common bus**, and a plurality of terminals coupled to the second interface portion for **connecting the second interface portion to the different types of memory chips via said common bus**.

Matsuda and Akamatsu, alone or in any combination, fail to teach at least the combination of, different types of memory chips connected to a common bus, and connecting the second interface portion to the different types of memory chips via the common bus. Matsuda merely teaches that a memory controller can be set to a selected one of a plurality of internal states depending on which type of memory is connected (see Matsuda, paragraph [0025]). Akamatsu is applied as allegedly teaching a semiconductor

system with a plurality of chips, wherein a terminal section is made up of terminal blocks and each terminal block is employed for connection with a respective subsidiary chip (see Office Action, page 4). However, Akamatsu fails to teach or suggest at least the combination of, different types of memory chips connected to a common bus, and connecting the second interface portion to the different types of memory chips via the common bus, and thus Akamatsu fails to cure the above-mentioned deficiencies of Matsuda.

With respect to Claim 26, Suzuki is cited as allegedly teaching an LSI with a plurality of circuit modules accessing data to a memory device on one LSI. However, Suzuki fails to cure the deficiencies of Matsuda and Akamatsu with respect to Claim 26.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. M.P.E.P. § 2143.03. For at least the reasons provided above, Applicants submit that Matsuda, Akamatsu, and Suzuki, alone or in any combination, do not teach or suggest all the elements of Claims 16 and 26. Accordingly, the Applicant submits that Claims 16 and 26 are allowable over the applied prior art.

With respect to Claim 18, Smith is applied in the claim rejection as allegedly teaching a configuration data set suitable for reconfiguring the programmable logic units which may be stored in a memory unit. With respect to Claim 19, Prouty is applied in the claim rejection as allegedly teaching a signaler translating command indications coming from command processor into the timing and assertion levels required as dictated by the chip specification. With respect to Claims 22 and 23, Takeda is cited as allegedly

teaching a function that informs the memories and the input/output circuits of which memory or input/output circuits are selected by the CPU and initiates the data transfer, the function being regarded as a chip enable control. With respect to Claim 25, Funaba is cited as allegedly teaching a memory module that has module data terminal pairs, a module command/address terminal pair, and a module clock terminal pair.

However, the Applicant respectfully notes that Smith, Prouty, Takeda, and Funaba, alone or in any combination, fail to teach or suggest at least the combination of features including a common memory controller capable of controlling different types of memory chips which are connected to a common bus, and a plurality of terminals coupled to the second interface portion for connecting the second interface portion to the different types of memory chips via said common bus, as recited in amended Claims 16 and 26. In other words, Smith, Prouty, Takeda, and Funaba fail to overcome or otherwise address the deficiencies of the applied prior art with regards to Claims 18, 19, 22, 23, and 25.

Claims 17-25 depend from Claim 16. The Applicant respectfully submits that these claims are allowable for at least the same reasons independent Claim 16 is allowable, as well as for the additional subject matter recited therein.

Further, new claim 27 also depends from independent Claim 16, and as such, the Applicant respectfully submits that claim 27 is likewise allowable for at least the same reasons Claim 16 is allowable, as well as for the additional subject matter recited therein.

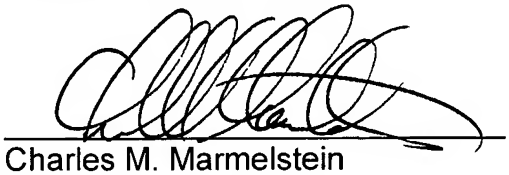
Conclusion

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding objections and rejections, allowance of Claims 16-27, and the prompt issuance of a Notice of Allowability are respectfully solicited.

Should the Examiner believe anything further is desirable in order to place this application in better condition for allowance, the Examiner is requested to contact the undersigned at the telephone number listed below.

In the event that this paper is not being timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to Counsel's Deposit Account Number 01-2300, referencing **Docket Number 108397-00109.**

Respectfully submitted,



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